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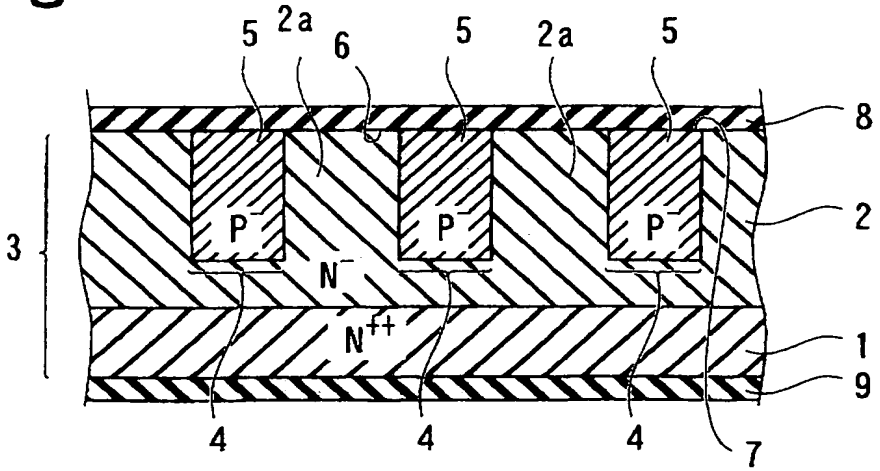
(54) Semiconductor device having a Schottky barrier diode structure

(57) Trenches are formed in the surface of a second semiconductor layer of a first conductivity type. A semiconductor filled material of a second conductivity type is filled in the trench. A Schottky metal electrode is formed on the surface of the second semiconductor layer and the surface of the semiconductor filled material. A Schottky junction is formed between the Schottky metal electrode and the second semiconductor layer. An ohmic contact is formed between the Schottky metal electrode and the semiconductor filled material. An avalanche breakdown voltage is increased when the impurity concentration of the second semiconductor layer and the semiconductor filled material and the interval between the trenches are set such that both the second semiconductor layer interposed between the semiconductor filled materials and the semiconductor filled material are completely depleted when the Schottky junction is reverse biased.

Fig. 1



EP 1 139 433 A1

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a semiconductor device, in particular, to a semiconductor device having a Schottky barrier diode structure.

2. Description of Related Art

[0002] While a Schottky barrier diode (SBD) has a low forward voltage and a high switching speed, the SBD has high reverse leakage current and a low reverse avalanche breakdown voltage as its disadvantage. In a medium or high voltage product of 100 V or higher, in particular, the reverse leakage current needs to be reduced to prevent thermorunaway. The impurity concentration of a drift region needs to be lowered so that a depletion layer is expanded while maintaining a high Schottky barrier height. As a result, forward characteristics are deteriorated.

[0003] Fig. 10 shows a structure for reducing leakage current by utilizing a pinch-off effect due to a junction used in a low voltage product. In this figure, an n-type semiconductor layer 2 (hereinafter, referred to as N^- epi-layer 2) having a low impurity concentration is formed on an n-type semiconductor substrate 1 (hereinafter, referred to as n-type substrate 1) having a high impurity concentration by epitaxial growth. P-type semiconductor regions 19 (hereinafter, referred to as P^+ regions 19) having a high impurity concentration are disposed at prescribed intervals in the main surface of the N^- epi-layer 2 by diffusion or embedding of polycrystalline silicon in the trench. An anode electrode film 8 contacted to the main surface 6 of the N^- epi-layer 2 and surfaces 20 of the P^+ regions 19 is formed. The anode electrode film 8 has Schottky contact with the main surface 6 of the N^- epi-layer 2. A cathode electrode film 9 having ohmic contact with the n-type substrate 1 is formed on the other surface of the n-type substrate 1.

[0004] When a reverse voltage is gradually applied to an SBD in Fig. 10, depletion layers 23_1 extend from side surfaces 21, 22 of the P^+ regions 19 into a region 2a in the N^- epi-layer 2 interposed between the adjacent P^+ regions 19 as shown in Fig. 11. When the reverse voltage is further applied, edges of the depletion layers extending from the side surfaces 21, 22 of the P^+ regions 19 come into contact with each other (pinch-off) and become one wide depletion layer 23_2. Therefore, an electric field applied to an interface between the main surface 6 of the N^- epi-layer 2 and the anode electrode film 8 is relaxed and thereby reverse leakage current can be reduced.

[0005] Fig. 12 shows a distribution of electric field strengths in a vertical direction along lines A and B, which are located at the centers of the P^+ region 19 and the N^- epi-region 2a interposed between the P^+ regions 19, respectively, when a reverse avalanche breakdown voltage is applied to the semiconductor device in a pinch-off state in Fig. 10. As described above, it is evident from Fig. 12 that an electric field applied to the interface between the main surface 6 of the N^- epi-layer 2 and the anode electrode film 8 is relaxed.

[0006] However, if the structure shown in Fig. 10 is applied to a medium or high voltage product of 100 V or higher, an electric field is increased at a pn junction between the bottom 24 of the P^+ region 19 and the N^- epi-layer 2, leading to deterioration of the reverse avalanche breakdown voltage. To maintain the reverse avalanche breakdown voltage, the impurity concentration of the N^- epi-layer 2 needs to be lowered, resulting in deterioration of forward characteristics.

[0007] There is also a structure in which only a bottom portion of the P^+ region 19 in Fig. 10 is formed of a p-type semiconductor region 25 having a low impurity concentration to relax the electric field at the bottom of the P^+ region 19 as shown in Fig. 13. However, if the impurity concentration of the p-type semiconductor region 25 becomes lower than a desired concentration, an electric field is concentrated at the bottom of the P^+ region 19, resulting in deterioration of the reverse avalanche breakdown voltage. If the impurity concentration of the p-type semiconductor region 25 is higher than a desired concentration, an electric field is concentrated at the bottom of the p-type semiconductor region 25, also resulting in deterioration of the reverse avalanche breakdown voltage.

[0008] In this structure, a large region having a low impurity concentration needs to be provided at the bottom to sufficiently relax the electric field. However, if a region having a low impurity concentration is further extended to under the p-type semiconductor region 25, a thickness of the N^- epi-layer 2 needs to be increased, resulting in deterioration of forward characteristics, which is a trade-off.

[0009] When reverse leakage current is reduced and a reverse avalanche breakdown voltage is maintained in a Schottky barrier diode with a medium or high avalanche breakdown voltage of 100 V or higher to prevent thermorunaway, there exists a trade-off that forward characteristics are deteriorated since the impurity concentration of the N^- epi-layer is lowered or a pinch-off effect due to the junction is utilized.

SUMMARY OF THE INVENTION

[0010] In view of the foregoing, an object of the present invention is to provide a semiconductor device such as a Schottky barrier diode or the like in which reverse leakage current is maintained at a conventional level while forward characteristics are greatly improved.

[0011] To achieve the above object, the present invention provides a semiconductor device having a first semiconductor layer composed of a semiconductor of a

first conductivity type, a second semiconductor layer of the first conductivity type having a lower impurity concentration than that of the first semiconductor layer, trench portions composed of thin trenches having a prescribed width and prescribed intervals therebetween formed in the second semiconductor layer surface, a semiconductor filled material composed of semiconductor of a second conductivity type, which is opposite to the first conductivity type, filled in the trench portions, a Schottky metal electrode formed on the surface of the second semiconductor layer and the surface of the semiconductor filled material while forming a Schottky junction with the second semiconductor layer and an ohmic contact with the semiconductor filled material, and an ohmic metal electrode formed on the surface of the first semiconductor layer. In this semiconductor device, at least the second semiconductor layer and the semiconductor filled material are constituted by the same semiconductor material. When an avalanche breakdown voltage BV_{AK} between the semiconductor filled material and the second semiconductor layer is expressed by

$$BV_{AK} = 60 \times (E_g/1.1)^{1.5} \times (N_d/10^{16})^{-3/4}$$

(where the unit of BV_{AK} is V; N_d represents an impurity concentration of the second semiconductor layer and its unit is cm^{-3}; and E_g represents an energy band gap value of the semiconductor material and its unit is eV), the width W_m between the semiconductor filled materials adjacent to each other formed in the second semiconductor layers satisfies the following equations (1) and (2):
(where the unit of the width W_m is cm; W_t represents a width

$$W_m \simeq \frac{W_t \times N_d}{N_a} \quad (1)$$

of the semiconductor filled material and its unit is cm; and N_a represents an impurity concentration in the semiconductor filled material and its unit is cm^{-3})

$$W_m \leqq \sqrt{\frac{2 \times \varepsilon_0 \times \varepsilon_s \times (BV_{AK}/n)}{q \times N_d}} \quad (2)$$

(where ε_s represents a relative permittivity of the semiconductor material; ε_0 represents a permittivity in vacuum and is 8.85418×10^{-14} F/cm; and q represents an elementary electrical charge and is 1.60218×10^{-19} coulomb; and in equation (2), $n > 1$).

[0012] The present invention also provides a semiconductor device in which an insulating film is formed on the sidewall and the bottom surface of the trench portion and the insulating film is disposed between the semiconductor filled material and the second semiconductor layer.

[0013] The present invention also provides a semiconductor device in which a high impurity concentration layer of the second conductivity type is formed on the surface of the semiconductor filled material.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014]

Fig. 1 is a schematic cross section showing one embodiment of the invention;
Fig. 2 is an explanatory view of the embodiment of the invention in operation;
Fig. 3 is an explanatory view of the embodiment of the invention in operation;
Fig. 4 is a graph showing characteristics of the electric field strength distribution in the embodiment of the invention;
Fig. 5 is a schematic cross section showing another embodiment of the invention;
Fig. 6 is a schematic cross section showing another embodiment of the invention;
Fig. 7 is a schematic cross section showing another embodiment of the invention;
Figs. 8(a) to 8(d) are cross sections showing processes of fabricating a device according to one embodiment of the invention;
Fig. 9 is a schematic plan view of a device according to the embodiment of the invention;
Fig. 10 is a schematic cross section of a conventional device;
Fig. 11 is an explanatory view of the conventional device in operation;
Fig. 12 is a graph showing characteristics of the electric field strength distribution of the conventional device; and
Fig. 13 is a schematic cross section of the conventional device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0015] Fig. 1 is a schematic cross section showing one embodiment of the present invention. This semiconductor device has a structure provided with a semiconductor substrate 3, a semiconductor filled material (P^- region) 5, a first electrode film (anode electrode film) 8, and a second electrode film (cathode electrode film) 9. The semiconductor substrate 3 is constituted by laminating a first semiconductor layer (n-type substrate) 1 of a first conductivity type and a second semiconductor layer (N^- epi-layer) 2 of the first conductivity type having a lower impurity concentration than that of the first layer. The semiconductor filled material (P^- region) 5 is obtained by filling polycrystalline silicon of a second conductivity type up to the same level as the surface of the

N^- epi-layer 2 in trenches 4 having a prescribed width formed at prescribed intervals in a surface of the N^- epi-layer 2 on one main surface side of this semiconductor substrate 3. The first electrode film (anode electrode film) 8 is composed of a metal which is brought into contact with both the surface 6 of the N^- epi-layer 2 and the surface 7 of the semiconductor filled material 5 and has Schottky junction with the surface 6 of the N^- epi-layer 2. The second electrode film (cathode electrode film) 9 forms ohmic contact with the n-type substrate 1 on the other main surface of the semiconductor substrate 3. In this semiconductor device, the impurity concentration of the semiconductor filled material 5 is so low that the whole semiconductor filled material 5 is depleted when a reverse voltage is applied to the pn junction between the N^- epi-layer 2 and the semiconductor filled material 5.

[0016] This embodiment will be described below with reference to Figs. 2 and 3. Figs. 2 and 3 are explanatory views of this embodiment of the invention in operation. First, when a reverse voltage starts to be applied to the semiconductor device, depletion layers 13, 14 extend from opposed sidewalls 11, 12 of adjacent trenches 4 to the N^- epi-region 2a interposed between the trenches 4 and the semiconductor filled material 5 in a lateral direction as shown in Fig. 2. When the reverse voltage is further applied, the width W_m between the adjacent trenches 4 formed in the surface of the N^- epi-layer 2 is preferably a width W_m which allows the depletion layers extending from the opposed sidewalls 11, 12 of the adjacent trenches 4 to be connected with each other.

[0017] The width W_m which allows the depletion layers extending from the adjacent trenches 4 to be connected with each other means a width W_m which also allows the whole N^- epi-region 2a interposed between the trenches 4 to be depleted when the whole semiconductor filled material 5 is depleted. This width W_m is related to the width W_t and the concentration N_a of the semiconductor filled material 5 formed in the trench 4 and the concentration N_d of the N^- epi-layer 2a. When an avalanche breakdown voltage BV_{AK} between the semiconductor filled material and the second semiconductor layer is expressed by

$$BV_{AK} = 60 \times (E_g/1.1)^{1.5} \times (N_d/10^{16})^{-3/4}$$

(where the unit of BV_{AK} is V; N_d represents an impurity concentration of the second semiconductor layer and its unit is cm^{-3}; E_g represents an energy band gap value of the semiconductor material and its unit is eV; when the semiconductor material is silicon, E_g is 1.12 eV, and when the material is GaAs, E_g is 1.43 eV.), the width W_m of between semiconductor filled materials adjacent to each other formed in the second semiconductor layers satisfies the following equations (1) and (2):

$$W_m \simeq \frac{W_t \times N_d}{N_a} \quad (1)$$

(where the unit of the width W_m is cm; W_t represents a width of the semiconductor filled material and its unit is cm; and N_a represents an impurity concentration in the semiconductor filled material and its unit is cm^{-3})

$$W_m \leqq \sqrt{\frac{2 \times \varepsilon_0 \times \varepsilon_s \times (BV_{AK}/n)}{q \times N_d}} \quad (2)$$

(where ε_s represents a relative permittivity of the semiconductor material; ε_0 represents a permittivity in vacuum and is 8.85418×10^{-14} F/cm; q represents an elementary electrical charge and is 1.60218×10^{-19} coulomb; and in equation(2), $n > 1$).

[0018] When the whole semiconductor filled material 5 is depleted, the whole N^- epi-region 2a is also depleted only under the condition under which these equations (1) and (2) are satisfied. That is, since both the semiconductor filled material 5 and the N^- epi-region 2a are depleted, one wide depletion layer 15 connected from the anode electrode film 8 to the bottom of the trench 4 is formed as shown in Fig. 3. When a reverse voltage is further applied, the voltage applied after formation of this wide depletion layer 15 is generally applied into this wide depletion layer 15. This wide depletion layer 15 is formed by depletion layers extending from the sidewalls 11, 12 of the trenches 4 in the lateral direction. At the point when the depletion layers 13 extending from the trenches 4 in the lateral direction are connected, the electric field in the depletion layer 15 is still low. When the reverse voltage is further applied, the electric field strength in the depletion layer 15 is increased as a whole. When the electric field strength reaches the critical value, breakdown starts. In case of a reverse avalanche breakdown voltage at the pn junction, breakdown occurs in the vicinity of the pn junction portion where the electric field strength becomes the highest. In the structure of the semiconductor device of the present invention, however, breakdown does not necessarily occur in the vicinity of the pn junction portion. The electric field strength of the pn junction can be sufficiently relaxed by forming the above-described depletion layer 15. The avalanche breakdown voltage may be reached at the center between the adjacent trenches 4 in the N^- epi-region 2a interposed between semiconductor filled material 5 before breakdown occurs in the vicinity of the pn junction portion.

[0019] It is preferable that the impurity concentrations N_d and N_a, the width W_t, and the width W_m satisfy the equation $W_m = W_t \times N_d/N_a$ but W_m can not be completely equal to $W_t \times N_d/N_a$ on practically manufactured devices. The symbol connecting the left-hand and the right-

hand side of the equation (1) means "approximately equal" and used here to include error arisen in manufacture which is within the range that does not affect avalanche breakdown voltage much.

[0020] As described above, a plurality of straight trenches having an approximate rectangular cross section are arranged in parallel and the equation (1) means that the total amount of the impurities disposed in a region between the adjacent trenches filled with the semiconductor material is approximately equal to the total amount of the impurities in one trench.

[0021] When the semiconductor filled material disposed in the trenches and the semiconductor material disposed in the region interposed between the trenches are reverse biased, depletion layers extend from two trenches facing to each other and being located at the both sides of the semiconductor material to the semiconductor material interposed between the trenches.

[0022] Equation (2) means that the depletion layers extending from the opposite sides of the semiconductor material come into contact in the semiconductor material disposed in the region interposed between the two trenches facing each other before the reverse bias voltage reaches the avalanche breakdown voltage of the semiconductor material and the avalanche breakdown voltage of the semiconductor filled material.

[0023] Fig. 4 shows the distribution of electric field strengths in a vertical direction along lines A and B, which are located at the centers of the semiconductor filled materials 5 and the N^- epi-region 2a interposed between the trenches 4, respectively, when a reverse avalanche breakdown voltage is applied to the semiconductor device in Fig. 1. As described above, the electric field strength in the depletion layer 15 is increased as a whole. The electric field strength in the depletion layer is increased with the same gradient as when the depletion layers 13 extending from the sidewalls 11, 12 of the trenches 4 are connected and depleted and becomes generally uniform in the depletion layer 15. There is no site where the electric field strength is particularly high. Therefore, when the N^- epi-layer 2 has such an impurity concentration N_d as to allow the depletion layers 13 extending from the sidewalls 11, 12 of the trenches 4 in the lateral direction to be connected, a reverse avalanche breakdown voltage can be increased without lowering the impurity concentration unlike a conventional structure product since the width of the depletion layer 15 can be further increased only by increasing the depth of the trench 4. Therefore, forward characteristics can be greatly improved while the electric field strength applied to the interface between the main surface 6 of the N^- epi-layer 2 and the anode electrode film 8 is maintained at the same level as that of a conventional structure product.

[0024] In the structure of the present invention, the reverse avalanche breakdown voltage can be determined only by changing the width of the depletion layer 15 extending downward from the anode electrode film 8. In other words, the reverse avalanche breakdown voltage is determined depending on the depth of the trench 4 having the semiconductor filled material 5 therein. Therefore, when the width W_m of the N^- epi-region 2a interposed between the trenches 4 and the impurity concentration in the N^- epi-layer 2 are set such that the depletion layers 13 extending from the trenches 4 in the lateral direction are connected, medium and high avalanche breakdown voltages can be obtained without lowering the impurity concentration of the N^- epi-layer 2 to increase a reverse avalanche breakdown voltage unlike a conventional structure product. That is, there is no increase in leakage current when a reverse voltage is applied and thereby forward characteristics can be greatly improved.

[0025] A method of fabricating a device of the present invention (Schottky barrier diode) will be described below with reference to Figs. 8(a) to 8(d). Figs. 8(a) to 8(d) are cross sections showing processes of fabricating the SBD.

[0026] First, a semiconductor substrate 3 is formed by laminating an N^- epi-layer 2 (phosphorus concentration $N_d = 1 \times 10^{16}$ atoms/cm^3) having a thickness of about 10 μm on an n-type substrate 1 (arsenic concentration 2×10^{19} atoms/cm^3) by epitaxial growth as shown in Fig. 8(a).

[0027] Subsequently, a silicon oxide film 18 is formed about 5000 x 10^{-8} cm on the surface of the N^- epi-layer 2 by thermal oxidation. Then, the silicon oxide film 18 is removed with a width W_t of about 0.6 μm and left with a width W_m of about 2.4 μm by photolithography resulting in stripes. By using this film as a mask, silicon of the N^- epi-layer 2 is etched with a gas to form trenches 4 of about 6 μm in depth from the surface of N^- epi-layer as shown in Fig. 8(b). At this time, n = 1.42 in the aforementioned equation (2).

[0028] Subsequently, polycrystalline silicon into which boron of N_a = about 4×10^{16} atoms/cm^3 is doped is deposited about 1 μm on the inner surface of the trenches 4 and on the surface of the silicon oxide film 18 as shown in Fig. 8(c) and then etched back until its height becomes the same level as the surface of the N^- epi-layer 2.

[0029] Subsequently, the silicon oxide film 18 used as a mask for forming trenches 4 is removed by etching. Schottky barrier metal is vapor deposited on the surface 6 of the N^- epi-layer 2 and the surface 7 of the polycrystalline silicon filled in the trenches 4 to form an anode electrode film 8. A cathode electrode film 9 is formed on the other side of the n-type substrate, which is a rear surface, and thus this embodiment of the invention is accomplished as shown in Fig. 8(d) (embodiments of the peripheral structure are omitted).

[0030] Figs. 5, 6 and 7 show structures of other embodiments of the invention. Fig. 5 is a cross section showing an example where an insulating film 16 is formed on the sidewalls 11, 12 and the bottom surface 10 of the trenches 4 in advance when polycrystalline sil-

icon (semiconductor filled material 5) having a low impurity concentration is filled in the trenches 4 and then a semiconductor filled material 5 is provided. This insulating film 16 plays a role of making leakage current almost 0 (zero) when a reverse voltage is applied between the polycrystalline silicon and the N^- epi-layer 2.

[0031] Fig. 6 shows an example where a fourth semiconductor region (P^{++} region) 17 of the second conductivity type having a high impurity concentration is provided so that the depletion layer 14 extending to the semiconductor filled material 5 when a reverse voltage is applied does not reach the surface 7 of the semiconductor filled material 5. This P^{++} region 17 can prevent leakage current which occurs because the depletion layer 14 formed upon application of a reverse voltage reaches the anode electrode film 8 brought into contact with the surface 7 of the semiconductor filled material 5 (punch through) and can make the potential of the semiconductor filled material 5 the same as that of the anode electrode film 8 by having ohmic contact with the anode electrode film 8 brought into contact with the surface 7 of the semiconductor filled material 5.

[0032] Furthermore, Fig. 7 shows a combination of the above-described structures, which is an example where an insulating film 16 is formed in the trenches 4 and then a P^{++} region 17 is formed on the surface of the semiconductor filled material 5.

[0033] Not polycrystalline silicon, but single crystal silicon of the second conductivity type may be formed by epitaxial growth to constitute the semiconductor filled material 5.

[0034] The reverse leakage current which occurs when the semiconductor filled material 5 is constituted by polycrystalline silicon can be reduced by forming p^--type single crystal silicon by epitaxial growth. This structure can also be applied to all the above-described structures.

[0035] As described above, in the present invention, a p^- region is provided in a trench formed in a surface of an N^- epi-layer. Since depletion layers extending from the pn junctions of side surfaces of the trenches are connected with each other in this P^- region and the N^- epi-layer region interposed between the trenches, a wide depletion layer from the surface to the bottom of the trench can be formed to increase a reverse avalanche breakdown voltage. Therefore, the reverse avalanche breakdown voltage can be increased only by changing the depth of the trench without changing an impurity concentration of the N^- epi-layer. Thus, a semiconductor device such as a Schottky barrier diode or the like in which forward characteristics can be greatly improved can be provided without changing reverse characteristics.

Claims

1. A semiconductor device comprising:

a first semiconductor layer composed of a semiconductor of a first conductivity type;
a second semiconductor layer of the first conductivity type having a lower impurity concentration than that of the first semiconductor layer;
trench portions composed of thin trenches having a prescribed width and prescribed intervals therebetween formed in the surface of the second semiconductor layer;
a semiconductor filled material composed of semiconductor of a second conductivity type, which is opposite to the first conductivity type, and filled in the trench portions;
a Schottky metal electrode formed on the surface of the second semiconductor layer and the surface of the semiconductor filled material, said Schottky metal electrode forming a Schottky junction with the second semiconductor layer and an ohmic contact with the semiconductor filled material; and
an ohmic metal electrode formed on the surface of the first semiconductor layer; said semiconductor device, wherein
at least said second semiconductor layer and said semiconductor filled material are constituted by the same semiconductor material;
when an avalanche breakdown voltage BV_{AK} between said semiconductor filled material and said second semiconductor layer is expressed by

$$BV_{AK} = 60 \times (E_g/1.1)^{1.5} \times (N_d/10^{16})^{-3/4}$$

(where the unit of BV_{AK} is V; N_d represents an impurity concentration of the second semiconductor layer and its unit is cm^{-3}; and E_g represents an energy band gap value of the semiconductor material and its unit is eV), the width W_m between the semiconductor filled materials adjacent to each other formed in the second semiconductor layer satisfies the following equations (1) and (2):

$$W_m \simeq \frac{W_t \times N_d}{N_a} \quad (1)$$

(where the unit of the width W_m is cm; W_t represents a width of the semiconductor filled material and its unit is cm; N_a represents an impurity concentration of the semiconductor filled material and its unit is cm^{-3})

$$W_m \leqq \sqrt{\frac{2 \times \varepsilon_0 \times \varepsilon_s \times (BV_{AK}/n)}{q \times N_d}} \quad (2)$$

(where ε_s represents a relative permittivity of the semiconductor material; ε_0 represents a permittivity in vacuum and is 8.85418×10^{-14} F/cm; q represents an elementary electrical charge and is 1.60218×10^{-19} coulomb; and in the equation (2), $n > 1$).

2. The semiconductor device according to claim 1, wherein an insulating film is formed on sidewall and bottom surface of the trench portion and the insulating film is disposed between said semiconductor filled material and said second semiconductor layer.

3. The semiconductor device according to claim 1, wherein a high impurity concentration layer of the second conductivity type is formed on the surface of the semiconductor filled material.

4. The semiconductor device according to claim 2, wherein a high impurity concentration layer of the second conductivity type is formed on the surface of the semiconductor filled material.

Fig. 1

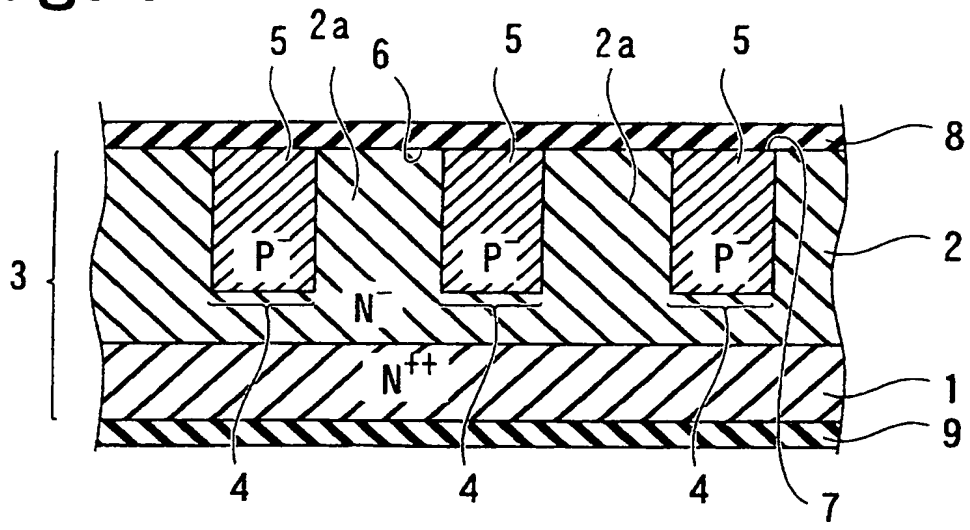


Fig. 2

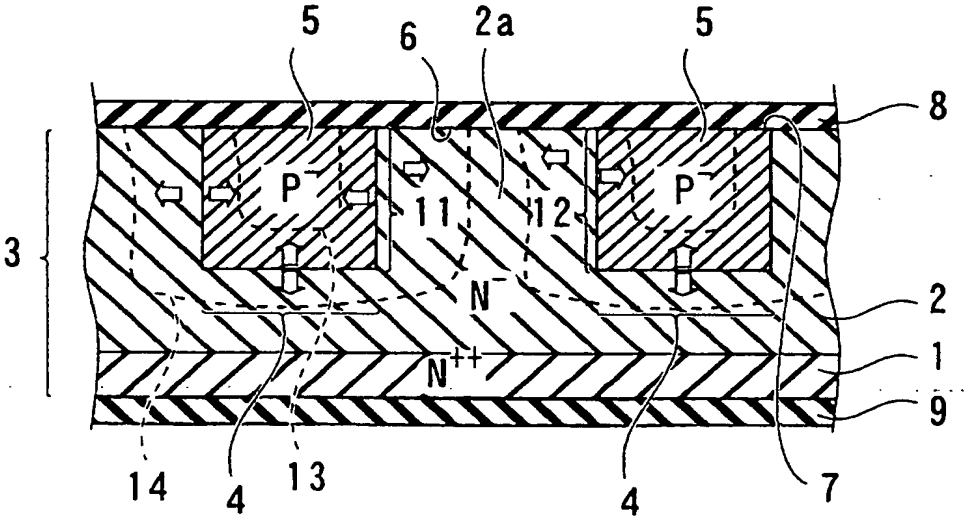
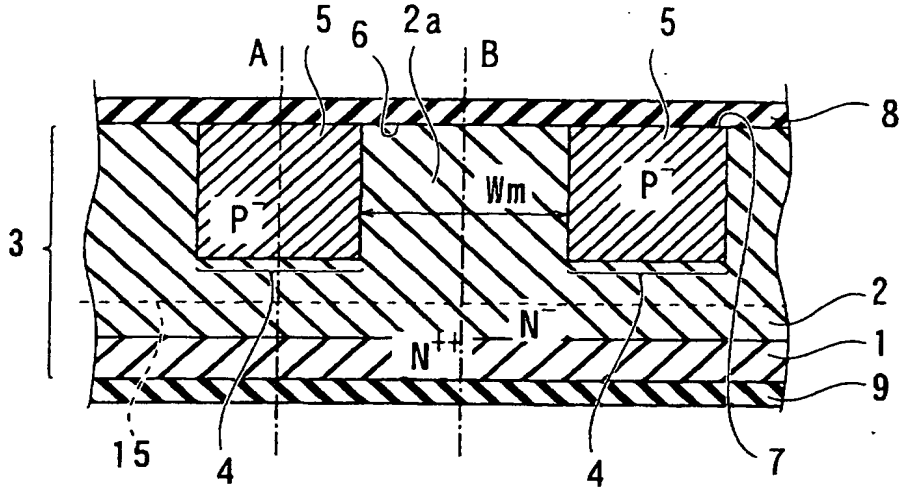


Fig. 3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8
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P
Wm
P
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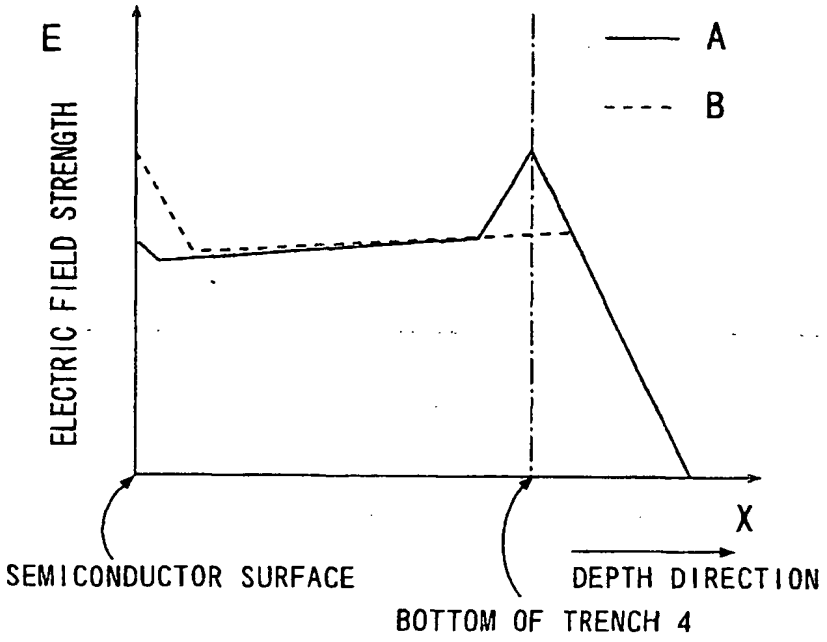
N
1
N++
9
15
4
4
7

Fig. 4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B
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X
SEMICONDUCTOR SURFACE
DEPTH DIRECTION
BOTTOM OF TRENCH 4

Fig. 5

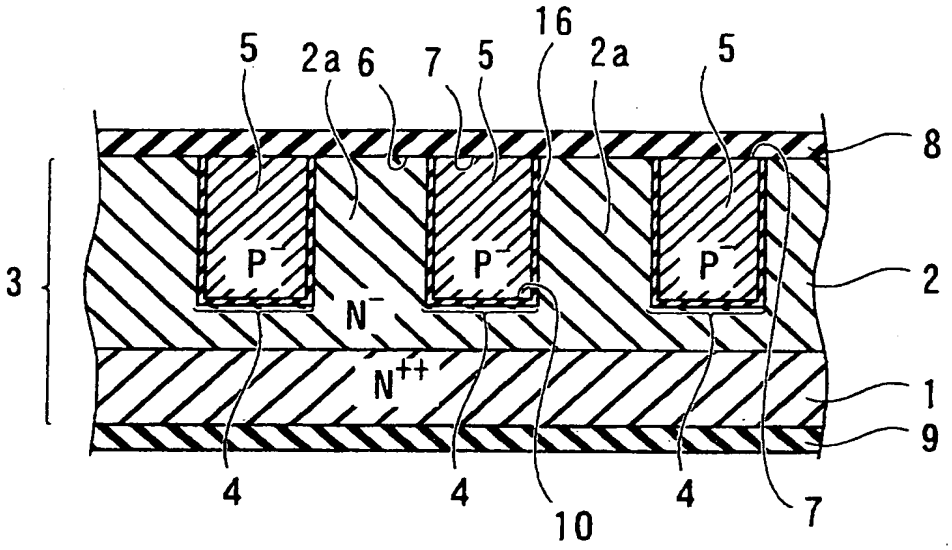
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Fig. 6

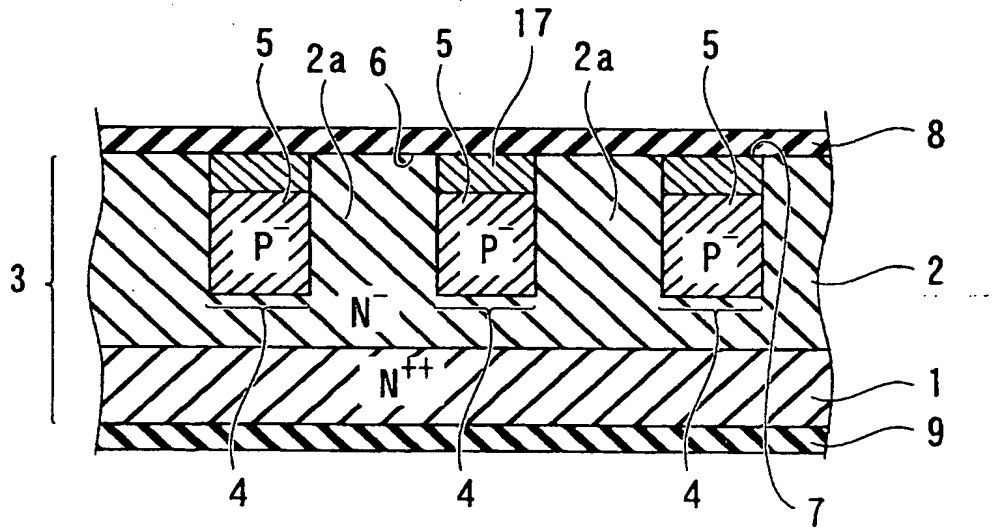
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Fig. 7

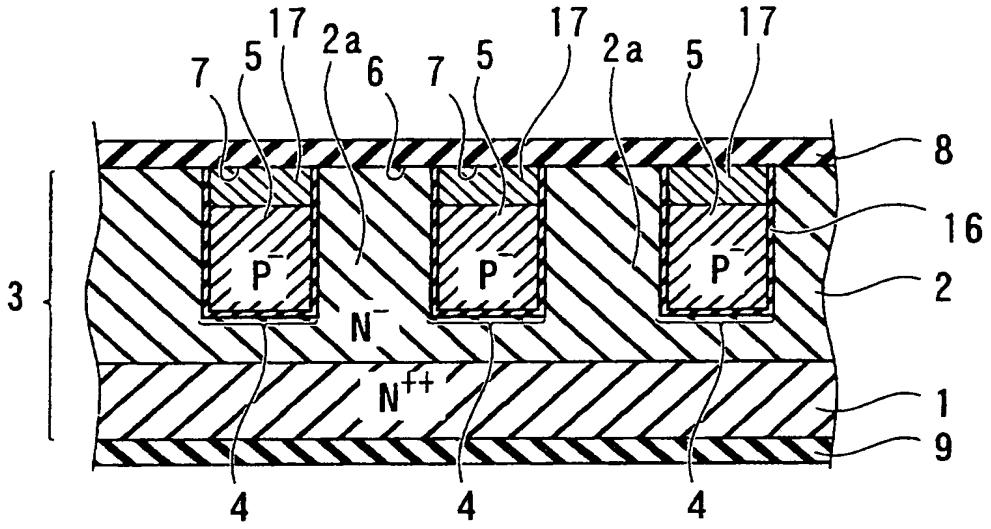


Fig. 8A

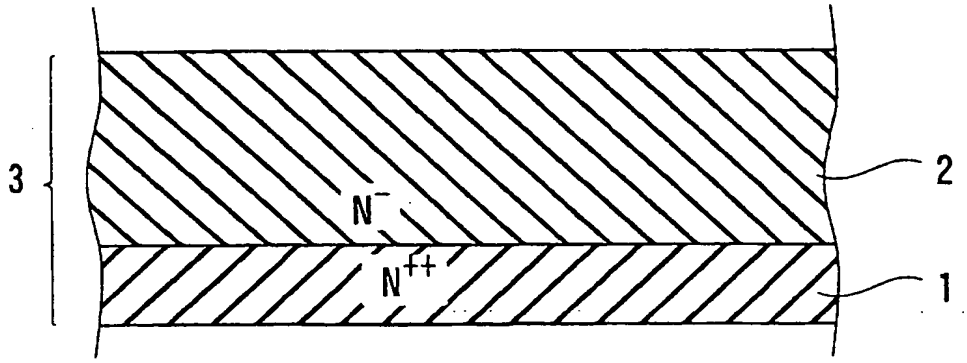


Fig. 8B

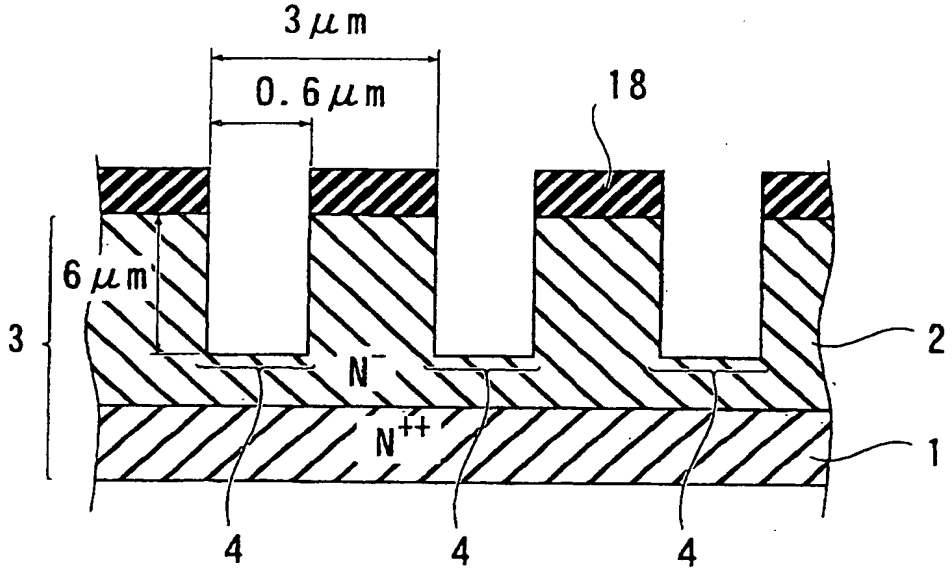


Fig. 8C

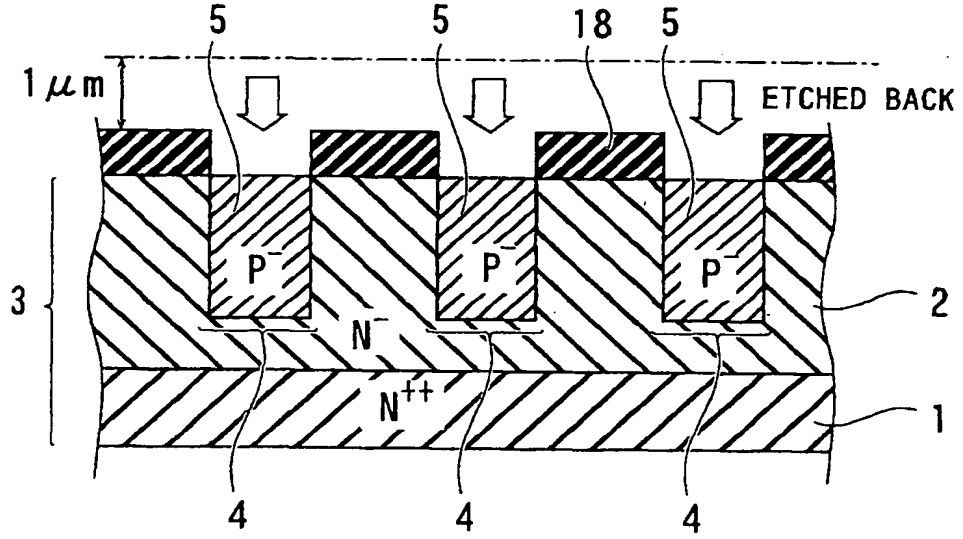


Fig. 8D

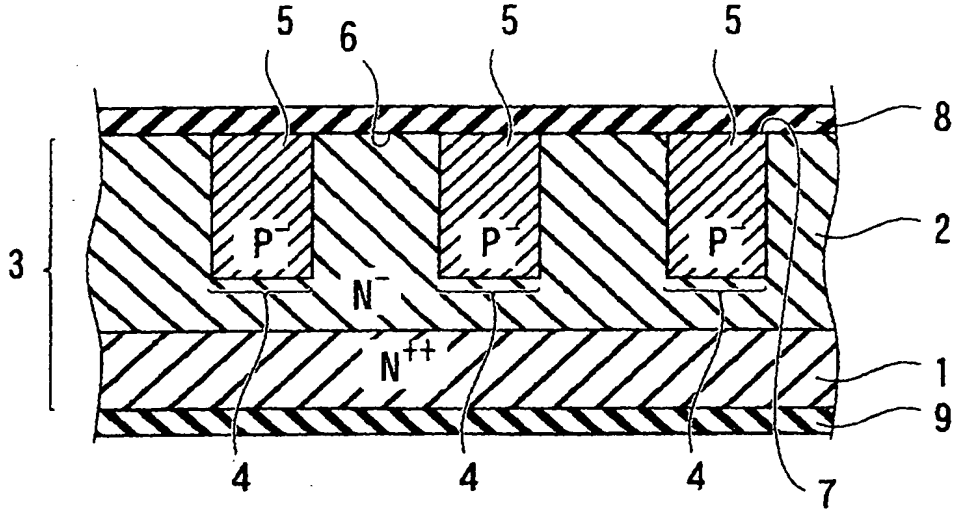


Fig. 9

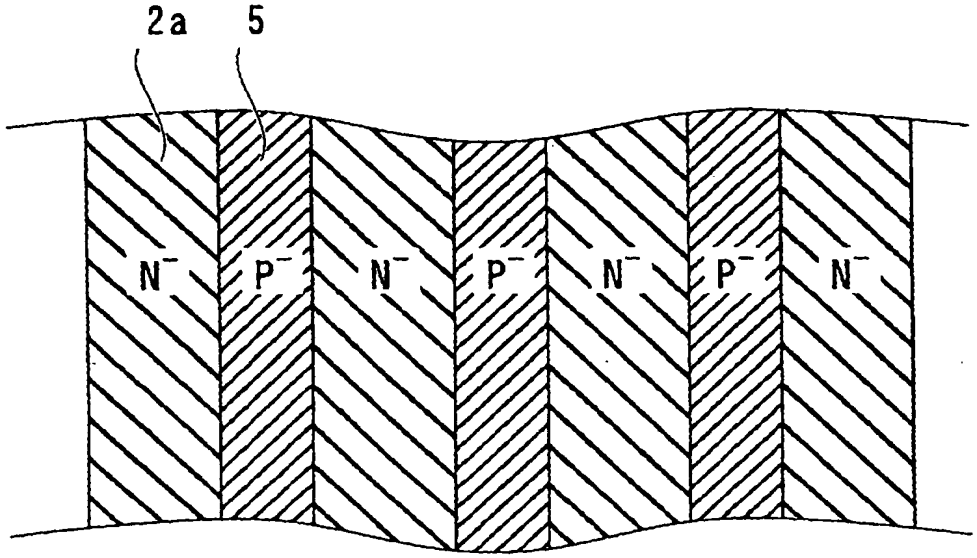


Fig. 10 PRIOR ART

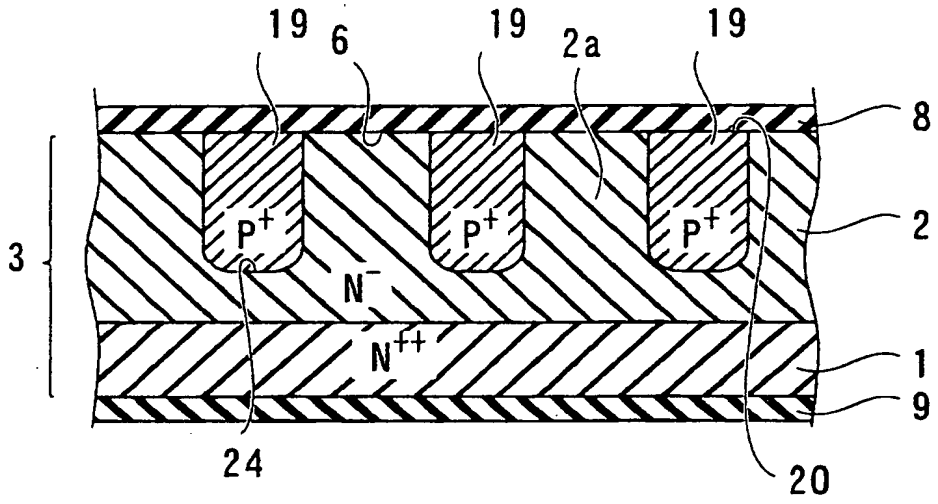


Fig. 11 PRIOR ART

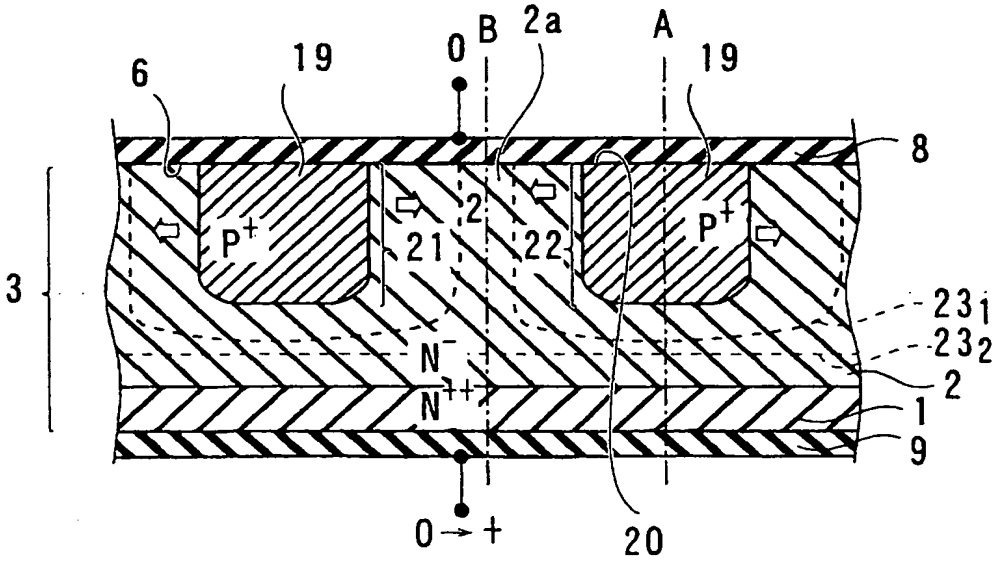


Fig. 12 PRIOR ART

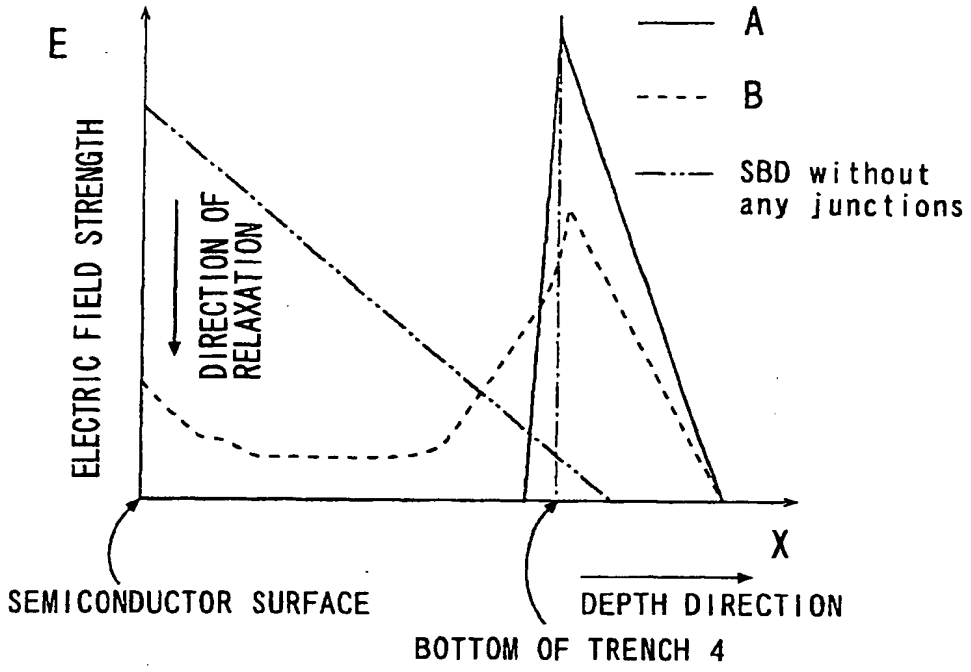
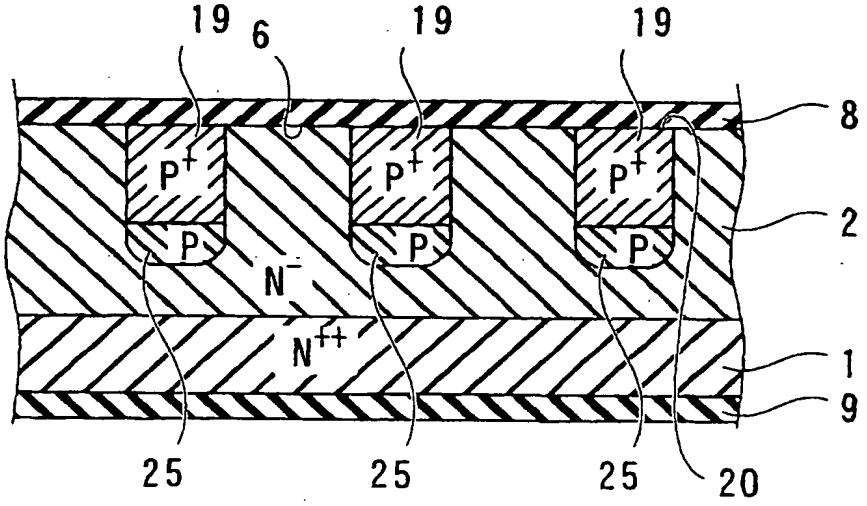


Fig. 13 PRIOR ART



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The present search report has been drawn up for all claims

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BERLIN	29 June 2001	Juhl, A

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